Abstract—Accounting for all possible short circuits in a direct current circuit can prove to be an arduous process. To avoid unintended operation and circuit damage, short circuit protection may be implemented via hardware or software. This paper views the short circuit detection problem as a hardware-software co-design problem in which an inductor installed in a DC circuit is designed alongside a microcontroller. Although short circuit detection is often a mission-critical process, we provide a framework depicting methods by which a short circuit may be detected by a microcontroller. Additionally, we establish the utilization requirement of the proposed methods and subsequently the remaining utilization under Uniprocessor EDF scheduling.

I. INTRODUCTION

Electronic circuits are often accompanied by a form of short circuit protection (e.g., a fuse, thermal breaker, or other device) which halts current flow when the current passing through the circuit is too high. This protection is placed to avoid currents that, when high enough, can cause damage to the circuit through joule heating. Additionally, some fuses, as a result of a short, must be replaced. This implementation of short circuit detection is rooted exclusively in hardware and may require maintenance. To provide an alternative method for short detection, we view the short detection problem a hardware-software co-design problem for which the implementation of a cyber-physical system provides a sound solution. The proposed solution relies on an inductor installed in a DC circuit which is designed alongside a microcontroller. The proposed solution detects short circuits through a safe, repeatable process by which a microcontroller operating under real-time constraints utilizes the properties of inductance to identify shorts in an electrical system.

Related works include the use of Zone Selective Interlocking on systems with alternating current as in [4] but not for DC. Similar in nature is the application of the Rogowski coil in [6] which is used to measure current but not restrict its rise using the inductive properties of the coil. In this work, we focus on direct current (DC) circuits where current rises are more rapid than alternating current (AC) and leverage the properties of the inductor to slow the current rise and detect the short. We also rely on the work of [1] and [2] to provide the accompanying real-time system model that relates processor utilization to the physical properties of the inductor thus allowing the reader to trade utilization for board space consumed.

Relying on the inductive properties of a DC resistor-inductor (RL) circuit and the earliest deadline first (EDF) schedulability of real-time tasks on preemptive uniprocessor systems, we propose that a short in a DC RL circuit may be detected through analysis of the rate of current rise and the process of detection modeled by a real-time periodic task. We propose that the relationship between real-time utilization of the processor and the spatial properties of the inductor may be established such that fixed parameters on either the software or hardware ends of the cyber-physical system may be used to provide optimal values for the opposite side of the relation.

Due to the interdisciplinary nature of this paper, a large electronics engineering background has been incorporated. This background information is not a contribution of the paper and serves only as context for the proposed solution. Section II provides an overview of the electronics background required to interpret the circuits provided and the nomenclature used. Section III provides basic information about the inductor and the laws within electronics that define the spatial properties of an inductor and, subsequently, its inductance. Section IV provides the first contribution of the paper a model for identifying the properties of the circuits analyzed and the association of the model with a real-time system task. Section V depicts methods of short detection given the constraints provided in our model. Section VI provides a real-time systems overview based on previous work not contributed by this paper. The resultant relationship provided at the end of section VI is contributory. Section VII provides the model optimization for both fixed board constraints and fixed real-time utilization as contributions from this paper.

We find the contributions of this paper to be surmised as the following:

1. Short detection methods for DC RL circuits.
2. An equivocation between inductor spatial parameters and real-time processor utilization under preemptive uniprocessor EDF scheduling.
3. A process for identifying inductor orientation and minimum spatial properties given a fixed real-time utilization under preemptive uniprocessor EDF scheduling.
4. A process for identifying minimum real-time utilization under preemptive uniprocessor EDF scheduling given fixed inductor spatial parameters.
II. ELECTRONICS BACKGROUND

To provide background for understanding the proposed model, the following section includes an overview of DC circuits, RL circuits, electronic nomenclature, Ohm’s law, and the definition of a short. This information is known, thoroughly researched and not a contribution of this paper. This section serves exclusively as a brief overview.

A. DC Circuits

Direct current (DC) circuits are circuits in which the direction of current flow does not change [5]. This current flow differs from AC electric power supplied to residential or industrial facilities where current flow switches back and forth. An example DC circuit is provided in Figure 1 depicting a voltage source with a single resistor.

![Fig. 1. An Example DC Circuit](image1)

B. Nomenclature

For the purpose of understanding the electronics background and the system model, the following nomenclature:

<table>
<thead>
<tr>
<th>Term</th>
<th>Symbol</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>V</td>
<td>Volt</td>
</tr>
<tr>
<td>Current</td>
<td>I</td>
<td>Ampere</td>
</tr>
<tr>
<td>Resistance</td>
<td>R</td>
<td>Ohm</td>
</tr>
<tr>
<td>Magnetic Field</td>
<td>B</td>
<td>Tesla</td>
</tr>
<tr>
<td>Magnetic Flux</td>
<td>Φ</td>
<td>Weber</td>
</tr>
<tr>
<td>Inductance</td>
<td>L</td>
<td>Henry</td>
</tr>
<tr>
<td>Electromotive Force</td>
<td>E</td>
<td>Volt</td>
</tr>
</tbody>
</table>

C. Ohm’s Law

To assist in mathematical modeling of DC circuits we introduce Ohm’s Law, a fundamental formula in electronics establishing the relationship between voltage, current, and resistance:

\[ V = IR \] (1)

where \( V \) is voltage, \( I \) is current, and \( R \) is resistance or impedance. Ohm’s law establishes that for a given voltage, an increase in resistance brings a decrease in current and vice versa. Equation (1) will be referenced frequently throughout the paper.

An example application can be computed using Equation (1) to determine the current flow through the DC circuit in Figure 1. It is known that \( V \) is 5 Volts and \( R \) is 1 Ohm. This gives:

\[ 5V = I \times 1\Omega \]

\[ I = 5A \]

D. Short

For the purposes of this paper, a short is defined as the flow of current through an alternate, unintended path in a circuit with little or no impedance. A short is not defined herein as unintended operation, malfunction, or dysfunctional operation of a circuit though it is possible for unintended operation to result from a short. To solidify this definition, we rely on Ohm’s law to identify the current incurred by a short using Figure 2 as an example.

![Fig. 2. A DC Circuit with a Short](image2)

Figure 2 depicts a short wherein the resistance of the centermost pathway is zero while the outermost pathway is non-zero. Since both resistors are supplied the same voltage, the resistors are considered to be in parallel. To find the combined resistance of resistors in parallel, we rely on the following equation:

\[ \frac{1}{R_{\text{Total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n} \] (2)

where \( R_i \) is the value of resistor at index \( i \) and \( n \) is the number of resistors in parallel. Applying Equation (2) to Figure 2 we may rearrange the equation to solve for \( R_{\text{Total}} \):

\[ \frac{1}{R_{\text{Total}}} = \frac{1}{R_1} + \frac{1}{R_2} \Rightarrow R_{\text{Total}} = \frac{R_1 \times R_2}{R_1 + R_2} \]

Filling in values from Figure 2 then gives:

\[ R_{\text{Total}} = 0 \times \frac{1}{1} = 0 \]

Applying Ohm’s law using the value \( R_{\text{Total}} \) as the resistance of the DC circuit we find:

\[ V = IR \]

\[ I = \frac{V}{R} \]

\[ I = \lim_{R \to 0} \frac{V}{R} = +\infty \]

This indicates that a short incurred with little or no impedance along the shorted path will produce theoretically infinite current.

E. Dangers of Shorts

Shorts in a DC circuit have the potential to cause unintended operation and thus unpredictable operation. In the best case, shorts are handled in hardware and allow the system to operate normally while the worst case is left to speculation. However, a known issue with shorts is joule heating. Per James’s Joule’s first law, Joule heating is the process whereby current through a conductor releases heat proportional to the square of the
current passing through the conductor. This may be modeled mathematically as:

\[ H \propto R I^2 t \]  

(3)

where \( H \) is heat energy released measured in joules, \( R \) is resistance, \( I \) is current, and \( t \) is time measured in seconds [3]. Joule heating may raise the temperature of the conductor to unsafe levels or physically degrade the conductor to the point of disconnection - producing an open in the circuit. This potential for permanent system damage serves as motivation to detect and mitigate damage from shorts.

\section*{F. RL Circuit}

A cornerstone of the model presented here is the DC RL circuit. The DC RL circuit is a DC circuit composed of resistors and inductors to which voltage is supplied. In the model to be presented, we rely on a first order RL circuit in which only one resistor and one inductor are used. An example RL circuit is provided in Figure 3.

\[ 5V \quad \begin{array}{c} \text{\footnotesize 1}\Omega \\ \text{\footnotesize 2H} \end{array} \]

Fig. 3. A DC RL Circuit

\section*{III. Inductor Basics}

\subsection*{A. Inductor Parameters}

When assessing the volume of an inductor, its spatial properties may be simplified as shown in Figure 4:

\[ A \quad \begin{array}{c} \text{\footnotesize N} \\ \text{\footnotesize l} \end{array} \]

Fig. 4. Inductor spatial parameters

In the figure above, \( N \) represents the number of completed turns in the inductor - in the case of the figure there are five (5) completed coils. \( A \) represents the area of a coil assuming all coils are of uniform area. \( l \) represents the length of the inductor from the beginning of the first coil to the end of the last coil. These properties correlate with the inductance of the inductor in the following formula:

\[ L = \frac{\mu_0 N^2 A}{l} \]  

(4)

The derivation of Equation (4) will be provided later in this section.

\subsection*{B. Types}

For the purpose of clarifying the assumptions of this paper, inductors are divided into two distinct types: air core and magnetic core. Air core inductors or air core coils are classified as inductors that do not contain a magnetic core. This refers to coils wound around a ceramic, plastic, or non-magnetic core. In contrast, magnetic core inductors contain cores composed of iron. Magnetic cores increase inductance and therefore allow our air core based model to serve as the worst case analysis of inductance provided for given inductor parameters.

\subsection*{C. Magnetic Field}

To validate the derivation of Equation (4), we provide the background information provided by the study of electromagnetism, namely magnetic fields and magnetic flux. A magnetic field is a vector field identifying the magnitude and direction of magnetic effect from electric currents or magnetic materials [5]. Magnetic fields for an air core inductor may be modeled using the equation:

\[ B = \frac{\mu_0 N l}{l} I \]  

(5)

where \( B \) is the magnetic field, \( \mu_0 \) is the permeability of free space measured as \( \frac{\text{tesla} \cdot \text{meter}}{\text{ampere}} \), \( N \) is the number of turns, \( l \) is the length of the solenoid in meters, and \( I \) is the current through the inductor. In our proposed model, the inductor used will have constant length and number of turns. Since the permeability of free space is defined as:

\[ \mu_0 = 4 \times \pi \times 10^{-7} \frac{\text{tesla} \cdot \text{meter}}{\text{ampere}} \]

this leaves \( I \) as the only variable in Equation (5) for our model.

\subsection*{D. Magnetic Flux}

Defined as the measure of magnetism passing through a given area, magnetic flux is the product of a magnetic field and the area of the surface it penetrates. This is defined by the equation:

\[ \Phi = BA \]  

(6)

where \( B \) is the magnetic field, \( A \) is the area the magnetic field penetrates measured in square meters, and \( \Phi \) is magnetic flux.

To combine and simplify these equations, we may substitute Equation (5) into Equation (6) to give:

\[ \Phi = \mu_0 \frac{N}{l} I A \]  

(7)
E. Faraday’s Law

Given Equation (7) we now use Faraday’s Law to relate magnetic flux to electromotive force. Faraday’s Law of induction predicts how an electromagnetic field produces electromotive forces (emf) through electromagnetic induction. Per Faraday’s Law, the electromotive force of an air core solenoid can be modeled as:

\[ E = -N \frac{\Delta \Phi}{\Delta t} \]  

(8)

where \( E \) is electromotive force, \( N \) is the number of turns, \( \Phi \) is the magnetic flux, and \( t \) is time measured in seconds. Recalling that the only variable in Equations (5), (6), and (7) is \( I \), we may substitute \( \Phi \) from Equation (7) into Equation (8) with the change in \( \Delta \Phi \) being \( \Delta I \). This gives:

\[ E = -\mu_0 N^2 A \frac{\Delta I}{\Delta t} \]  

(9)

F. Lenz’s Law

In addition to Faraday’s Law, Lenz’s Law states that an induced current flows in the direction opposite the current that produced it. This is identified in the Equation (8) and in the following equation for inductance by the negative sign preceding the equation body:

\[ E = -L \frac{\Delta I}{\Delta t} \]  

(10)

where \( E \) is electromotive force, \( N \) is the number of turns, \( \Phi \) is the magnetic flux, and \( t \) is time measured in seconds.

By equating Equations (9) and (10), we may solve for \( L \) to define a relationship between the inductance of an inductor and its spatial parameters:

\[ -L \frac{\Delta I}{\Delta t} = E = -\mu_0 N^2 A \frac{\Delta I}{\Delta t} \Rightarrow L = \frac{\mu_0 N^2 A}{l}. \]  

(11)

We rely on Equation (11) to act as the function by which board space may be optimized for inductance and as a cornerstone for real-time analysis.

G. Current as a Function of Time

As previously mentioned, Lenz’s Law states that induced current flows in the direction opposite the current that produced it. Because of this property, the current through an inductor cannot change instantaneously from zero to the final current value defined by Ohm’s Law in Equation (1). Instead, current through an inductor approaches \( \frac{V}{R} \) asymptotically as modeled by the equation:

\[ I(t) = \frac{V}{R} (1 - e^{-t/R}) \]  

(12)

where \( I \) is current, \( V \) is a constant voltage to the circuit containing the inductor, \( R \) is resistance, \( L \) is inductance and \( t \) is time measured in seconds. Notice that taking the limit as \( t \) approaches infinity of Equation (9) gives:

\[ \lim_{t \to \infty} I(t) \Rightarrow \lim_{x \to \infty} \frac{V}{R} (1 - e^{-t/R}) = \frac{V}{R} \]  

(13)

indicating that current approaches \( \frac{V}{R} \) and thus conforms to Ohm’s law.

Thus far, Equation (11) indicates that variations in the physical size of an inductor correlate with its inductance. From Equation (13) we know the current at time \( t \) is not only dependent on supplied voltage and resistance but also inductance since an increase in the value of \( L \) will decrease the time \( \frac{V}{R} \). In conjunction, this indicates that variations in the physical parameters of an inductor correlate with the time taken to approach \( \frac{V}{R} \) for a given DC RL circuit.

H. Mounting Orientations

Before analyzing the space consumed by inductors, we observe two possible orientations in which an inductor may be mounted to a printed circuit board (PCB). One mounting orientation is such that the inductor coils extend perpendicular to the face of the PCB as depicted in Figure 5. The shaded region indicates the board space consumed. We will hereafter refer to this orientation as **perpendicular mounting**.

![Fig. 5. Perpendicular Mounting.](image)

Another mounting orientation we define as **parallel mounting** such that the inductor coils extend parallel to the face of the PCB as depicted in Figure 6.

![Fig. 6. Parallel Mounting.](image)

I. Board Space Consumed

For each mounting orientation, different formulas can be derived for modeling the board area consumed with regard to length and area of the inductor.
1) Perpendicular Mounting: In perpendicular mounting, the board area consumed is defined as:

\[ A_{\text{perpendicular}} = \frac{4}{\pi} A \]  

(14)

where \( A \) is the area of the inductor coil from Equation (4). The height of the inductor \( h \) is equivalent to \( l \) from Equation (4) thereby producing an inductor volume \( V_{\text{inductor}} \) of:

\[ V_{\text{inductor}} = l \frac{4}{\pi} A \]  

(15)

2) Parallel Mounting: In parallel mounting, the board area consumed is defined as:

\[ A_{\text{parallel}} = l \cdot 2 \sqrt{\frac{A}{\pi}} \]  

(16)

where \( A \) is the area of the inductor coil from Equation (4). The height of the inductor \( h \) is no longer equivalent to \( l \) from Equation (4) as the length of the inductor is parallel to the board. Instead, \( h \) is defined as:

\[ h_{\text{parallel}} = 2 \sqrt{\frac{A}{\pi}} \]  

(17)

The volume for parallel mounting is equivalent to that of perpendicular mounting.

IV. SYSTEM MODEL

Relying on the aforementioned background information, we propose a system model composed of three primary components:

1. A DC RL Circuit that utilizes the properties of an inductor to slow current rise time via inductance. This system relates board space consumed by the inductor to its inductance.
2. An Operating Current Model (OCM) to identify the maximum operating current of the system and the critical current at which circuit damage occurs. This model determines the difference between the maximum current and critical current thereby determining the minimum time required for a short to cause current rise between the two values.
3. A real-time system periodic task utilization analysis under uniprocessor EDF scheduling to determine the remaining utilization on the processor handling short circuit detection. Using the minimum time from the previous component, the real-time model closes the relation of board space to processor utilization.

A. The DC RL Circuit

As previously mentioned, a DC RL circuit is one containing both a resistor and inductor. Our model assumes a first order RL circuit in which only one resistor and one inductor are present aside from the voltage supply. Figure 7 depicts a first order DC RL circuit used in this model where a short has already been placed.

B. Operating Current Model

Although our model uses a single form of DC RL circuit, circuits appear in many forms and for the purposes of this paper require a uniform framework by which the operating currents and other attributes of the circuit may be analyzed. Hereafter, circuits are modeled in the following manner:

\[ C = (\Gamma_I, I_{\text{crit}}) \]  

(18)

where \( C \) is the circuit described using parameters \( \Gamma_I \) and \( I_{\text{crit}} \). \( \Gamma_I \) is defined such that:

\[ \Gamma_I = (\gamma_0, \gamma_1, ..., \gamma_n) \]  

(19)

\[ \gamma_n = (I, V) \]  

(20)

Here \( \Gamma_I \) is composed of \( n \) operating current sets \( \gamma_i \) where \( i \) is the index of an operating current set. Each operating current set is a 2-tuple comprised of an operating current \( I \) and operating voltage \( V \). Only \( I \) and \( V \) are needed as Ohm’s Law will solve for the resistance \( R \) of each operating current set. Voltage and resistance are not assumed as the application of transistors may alter the impedance of a circuit and thus not require a change in voltage to alter current. Similarly, change in voltage supply without altering the circuit would result in steady impedance but an altered current.

\( I_{\text{crit}} \) is defined as the critical current of the system as determined by the user. The critical current represents the current value at which the system physically degrades or, in practice, the current value the user wishes to avoid reaching.

A final derivable parameter \( I_{\text{max}} \), is extracted from the OCM as follows:

\[ I_{\text{max}} = \max_{i \in \Gamma_I} \{\gamma_i\} \]  

(21)

Note that should \( I_{\text{crit}} \) be equivalent to \( I_{\text{max}} \), any current flow over \( I_{\text{max}} \) is assumed to be damaging and thus damage may not be prevented through this short detection model.

V. SHORT DETECTION METHODS

Detecting the short in the DC RL circuit provided by Figure 7 is possible via two methods presented here: utilizing the maximum operating current or the maximum derivative of current with respect to time \( \frac{dI}{dt_{\text{max}}} \). The former relies on the OCM to find the maximum operating current while the latter relies on the properties of an inductor.
A. Maximum Operating Current

One method of identifying a short in a DC circuit modeled using operating current sets is to remove power from the circuit when a current is detected above $I_{\text{max}}$. When an Analog-to-Digital Converter (ADC) returns a value above $I_{\text{max}}$ after taking into consideration the ADC tolerance, power to the system should be removed such that supplied voltage $V$ across the system becomes zero. A current above $I_{\text{max}}$ is indicative of malfunction and potentially a short which has forced the current flow to rise above the maximum expected operating current.

B. Maximum $\frac{dI}{dt}$

Another method of detection requires observing the rate of change of current. From (13) it is known that given a constant voltage and resistance, current will approach and converge to $\frac{V}{R}$. During convergence, the slope of $\frac{dI}{dt}$ approaches zero. Given the known inductance of the inductor, the derivative of (12) will provide the value of $\frac{dI}{dt}$ at any given time. Deriving (12) gives:

$$\frac{\partial}{\partial t} I(t) = \frac{\partial}{\partial t} \left( \frac{V}{R} (1 - e^{-\frac{t}{L}}) \right)$$

$$= \frac{V}{R} \frac{\partial}{\partial t} \left( 1 - e^{-\frac{t}{L}} \right)$$

$$= \frac{V}{R} \frac{ \partial }{ \partial t } e^{-\frac{t}{L}}$$

$$\frac{dI(t)}{dt} = \frac{V}{L} e^{-\frac{t}{L}}$$

$$\frac{dI(t)}{dt} = \frac{V}{L} e^{-\frac{t}{L}}$$

(22)

With $t$ being the only variable in (22), the greatest possible values of $\frac{dI}{dt}$ occurs at $t = 0$ and $R = 0$ while excluding infinite inductance ($L = +\infty$). This maximum value of $\frac{dI}{dt}$ is deemed

$$\frac{dI}{dt}_{\text{max}} = \frac{V}{L}$$

(23)

Given that (22) may only occur at $t = 0$ and $R = 0$, these scenarios occur when voltage is first applied and current has not begun to flow and when no impedance is encountered such as in a shorted RL circuit as depicted in Figure 7. Since all non-superconducting materials will provide some (often negligible) impedance, $\frac{dI}{dt}$ should never reach $\frac{V}{L}$. It is possible for an ADC sampling to occur at $t = 0$ at which point $\frac{dI}{dt}$ may be $\frac{V}{L}$. However, consecutive ADC samples reading $\frac{dI}{dt}_{\text{max}} = \frac{V}{L}$ would indicate $R \approx 0$ and therefore a short has taken place. Note that unlike using $I_{\text{max}}$ to determine the presence of a short, using $\frac{dI}{dt}_{\text{max}}$ allows for short detection before $I_{\text{max}}$ has been reached. It is possible for a short to occur at an operating current level below $I_{\text{max}}$ and for current rise to reach $\frac{dI}{dt}_{\text{max}}$ before $I$ exceeds $I_{\text{max}}$.

1) Minimum Time to Detection: Although using $\frac{dI}{dt}$ to detect a short is possible, a valuable detection occurs before critical current levels are reached. Per the OCM, this requires that enough samples occur in the time taken for current to rise from $I_{\text{max}}$ to $I_{\text{crit}}$. This length of time is deemed the minimum time to detection where

$$t_d = \frac{I_{\text{crit}} - I_{\text{max}}}{V/L}$$

(24)

This time frame signifies the worst case as it the time taken for current to rise from the maximum of all operating currents ($I_{\text{max}}$) to the critical current ($I_{\text{crit}}$) under the assumption that no resistance ($R = 0$) is encountered during the short. This worst case time span is only achievable in a DC RL circuit where the current flow is shorted via a superconductor with no resistance.

VI. REAL-TIME SYSTEM MODEL

Thus far, the spatial properties of an inductor have been related to its inductance. Thereafter, inductance is found to determine the maximum possible current rise at any given time $\frac{V}{L}$ and subsequently the shortest time span over which a short would need to be detected. Using the minimum time to detection $t_d$, we may not produce a real-time system model. Before doing so, we present established background information on real-time systems task modeling.

A real-time system is one in which the correctness of a computation has a logical and temporal component. The utility of computational results depends on the computational result itself and the time at which it is produced [1]. Here we rely on two components from real-time systems: the periodic task model and uniprocessor EDF scheduling.

A. Periodic Task Model

In real-time systems, periodic tasks are defined by an offset $a$, execution requirement $e$, a relative deadline $d$, and a period $p$. The offset identifies when the first job in the periodic task set is release. The execution requirement identifies the maximum execution time required by the task. The relative deadline is the time between each arrival and deadline of a job produced by the periodic task. The period is the time between successive job arrivals. We use the periodic task model to produce a short circuit detection task [1].

The worst case time to detection may be converted into a real-time periodic task $T_{sc} = (a_i, e_i, d_i, p_i)$ with the following parameters

$$a_i = 0$$

(25)

$$e_i = \text{user-defined}$$

(26)

$$d_i = p_i$$

(27)

$$p_i = \frac{t_d}{2}$$

(28)

where $a_i$ is the offset, $e_i$ is the execution time in seconds, $d_i$ is the relative deadline in seconds, and $p_i$ is the period in seconds. Assessing the architecture of different processors and ADCs chosen to monitor the DC RL circuit is left to the reader. Thus, the resultant execution time for sampling the ADC and calculating current in software is not assessed here but identified as $e_i$. 
B. Preemptive Uniprocessor EDF Scheduling

With the periodic task \( T_{sc} \) defined, we assess utilization on a preemptive uniprocessor under EDF Scheduling. According to \([2]\), a set of periodic tasks is schedulable with EDF if and only if:

\[
\sum_{i=1}^{n} \frac{e_i}{p_i} \leq 1
\]

where \( i \) is the index of a task in the set, \( e_i \) is the execution time and \( p_i \) is the period. Equation (29) establishes that the utilization cannot exceed 100% \([2]\). Since we use a single task this makes the utilization for \( T_{sc} \):

\[
U(T_{sc}) = 2 \frac{e_i}{l_d}
\]

The execution requirement is doubled as it is assumed two ADC samples are needed to determine \( \frac{V}{l} \). Given a known utilization for \( T_{sc} \) this allows for the computation of remaining utilization:

\[
U_{\text{remain}} = 1 - 2 \frac{e_i}{l_d}
\]

\[
U_{\text{remain}} = 1 - \left( \frac{2e_i}{I_{\text{crit}} - I_{\text{max}}} \cdot \frac{l}{\mu N^2 A} \right)
\]

Using (32) a relationship is established between the spatial components of the inductor and the utilization of the corresponding short circuit detection task.

VII. MODEL OPTIMIZATION

Having established the relationship between the board space consumed by an inductor and the real-time utilization under EDF schedulability, we propose an optimal solution for fixed values on either end of the relationship. Given a fixed utilization we propose a minimized board space consumption and given a fixed allowable board space we propose a minimized real-time utilization. Before optimization analysis of the model, we clarify and explain two key points: the assumption of constant turn density and the optimal inductor orientation.

A. Assumption of Constant Turn Density

Equation (4) shows contains the term \( \frac{N}{\gamma} \) which is referred to as turn density. It is important to note that purely elongating an inductor by extending \( l \) in Figure 4 will not increase inductance but instead decrease it. Turn density must stay constant with an increase in length for inductance to increase. Thus if an inductor is to be extended an from length \( l \) to \( 2 \cdot l \), the number of turns \( N \) should be doubled to \( 2 \cdot N \) accordingly to maintain turn density. This doubling would result in the inductance of this hypothetical inductor to be:

\[
L = \frac{\mu_0 (2 \cdot N)^2 A}{2 \cdot l} = \frac{\mu_0 \cdot 4 \cdot N^2 A}{2 \cdot l} = 2 \cdot \mu_0 N^2 A \frac{l}{l}
\]

To assist in optimization, we assume the turn density remains constant such that an increase in \( l \) gives an identical increase in \( N \).

B. Optimal Inductor Orientation

To find the inductor orientation providing the highest inductance for a given space, we must consider two constraints:

1. The area \( A \) from Equation (4) requires a square area with regard to board space. That is, the plane on which \( A \) rests is square.
2. The board space allowed must be defined in three dimensions: a length \( l \), width \( w \), and height \( h \).

Assuming the allowable board space is defined as a 3-tuple \((l, w, h)\), the optimal orientation for an inductor is as follows: Given three dimensions, a length, width, and height, the two dimensions whose minimum squared multiplied by the third dimension produce the largest volume form the plane to which the inductor coil mounting is perpendicular.

For example, provided the following 3-tuple: \((3, 2, 1)\) three pairs of dimensions may be selected and the square minimums are given:

A. \((3, 2)\) \(\Rightarrow (\min(3, 2))^2 = 4 \Rightarrow 4 \cdot 1 = 4\)

B. \((3, 1)\) \(\Rightarrow (\min(3, 1))^2 = 1 \Rightarrow 1 \cdot 1 = 1\)

C. \((2, 1)\) \(\Rightarrow (\min(2, 1))^2 = 1 \Rightarrow 1 \cdot 3 = 3\)

Set \( A \) produces the largest volume meaning the plane formed by dimensions \( l \) and \( w \) of unit length 3 and 2 respectively is the plane to which the inductor coils should be perpendicular. The other pairs of dimensions produce volumes less than the paired dimensions \((l, w)\). In this example, the coils are perpendicular to the plane formed by the length and width thus making the optimal inductor orientation parallel mounting.

C. Assumed OCM and Execution Requirement

To fill in the parameters which would be provided a priori, we rely on an assumed OCM and execution requirement leaving the inductor parameters and utilization requirement undefined for the purpose of analysis.

The assumed OCM is defined as:

\[
C = (\Gamma_I, 10A)
\]

\[
\Gamma_I = (\gamma_0)
\]

\[
\gamma_0 = (5A, 5V)
\]

We assume an execution time \( e_i \) of 1 \( \mu s \) to sample the ADC and calculate current flow.

D. Fixed Board Constraints

The first approach to optimization is made wherein the board space is fixed. This relies on the aforementioned optimal inductor orientation. Suppose allotted board space is restricted to the 3-tuple \((15\, \text{mm}, 10\, \text{mm}, 5\, \text{mm})\). For this 3-tuple, the optimal inductor orientation is such that the length \((15\, \text{mm})\) and width \((10\, \text{mm})\) form the plane to which the coil direction is perpendicular. Using Equation (14) this indicates the 15mm-10mm area comprises \(A_{\text{perpendicular}}\) and the 5mm dimension is defined as the inductor length \( l \). Solving Equation (14) for the area of the inductor \( A \) gives:

\[
A = \frac{\pi}{4} A_{\text{perpendicular}} = \frac{\pi}{4} \cdot 150\, \text{mm}^2
\]
Converting these values to meters and applying Equation (32) gives the remaining utilization provided by the maximum sized inductor that can fit within the board constraints:

\[
U_{\text{remain}} = 1 - \left( 2 \cdot 1 \times 10^{-6} \text{s} \cdot 5 \text{V} \cdot \frac{0.005 \text{m}}{\mu_0(N)^2 \cdot \frac{\pi}{4} \cdot 1.5 \times 10^{-4} \text{m}^2} \right)
\]

where \(\mu_0\) is defined as:

\[
\mu_0 = 4 \times \pi \times 10^{-7} \text{ tesla \cdot meter/ampere}
\]

This utilization remaining is the maximum remaining utilization assuming a smaller sampling period is not chosen. We leave the number of turns \(N\) to be decided by the reader.

E. Fixed Utilization

The second approach to optimization is made by fixing the utilization allowed for the short detection process. Suppose the allotted utilization is 0.25. Relying on Equation (30) we find the minimum time to detection \(t_d\) is solved as:

\[
t_d = 2 \frac{e_i}{U(T_{sc})} = 2 \frac{1 \times 10^{-6} \text{s}}{0.25} = 8 \times 10^{-6} \text{s}
\]

From Equation (24) we find:

\[
L = \frac{V}{I_{\text{crit}} - I_{\text{max}}} \cdot t_d = \frac{5 \text{V}}{10 \text{A} - 5 \text{A}} \cdot 8 \times 10^{-6} \text{s} = 8 \times 10^{-6} \text{H}
\]

This result indicates that, given the presented assumptions, the inductor used in the DC RL circuit must have inductance of at least \(8 \times 10^{-6} \text{H}\). An inductor with inductance greater than \(8 \times 10^{-6} \text{H}\) will provide a larger window for time to detection and allow for a lower utilization \(U(T_{sc})\).

VIII. CONCLUSION

In this paper, an cyber-physical system is modeled in which the inductive properties of a DC RL circuit are leveraged to construct a real-time periodic task which relies on rate of change of current to detect shorts in an electronic system. A relationship is established between utilization on a preemptive uniprocessor under EDF schedulability and the board space consumed by the inductor placed in-circuit.

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